**Lab Assignment 2 (20 Marks)**

**Show the output to instructor on 2/11/2020 (First Verification) and 4/11/2020 (Second Verification)**

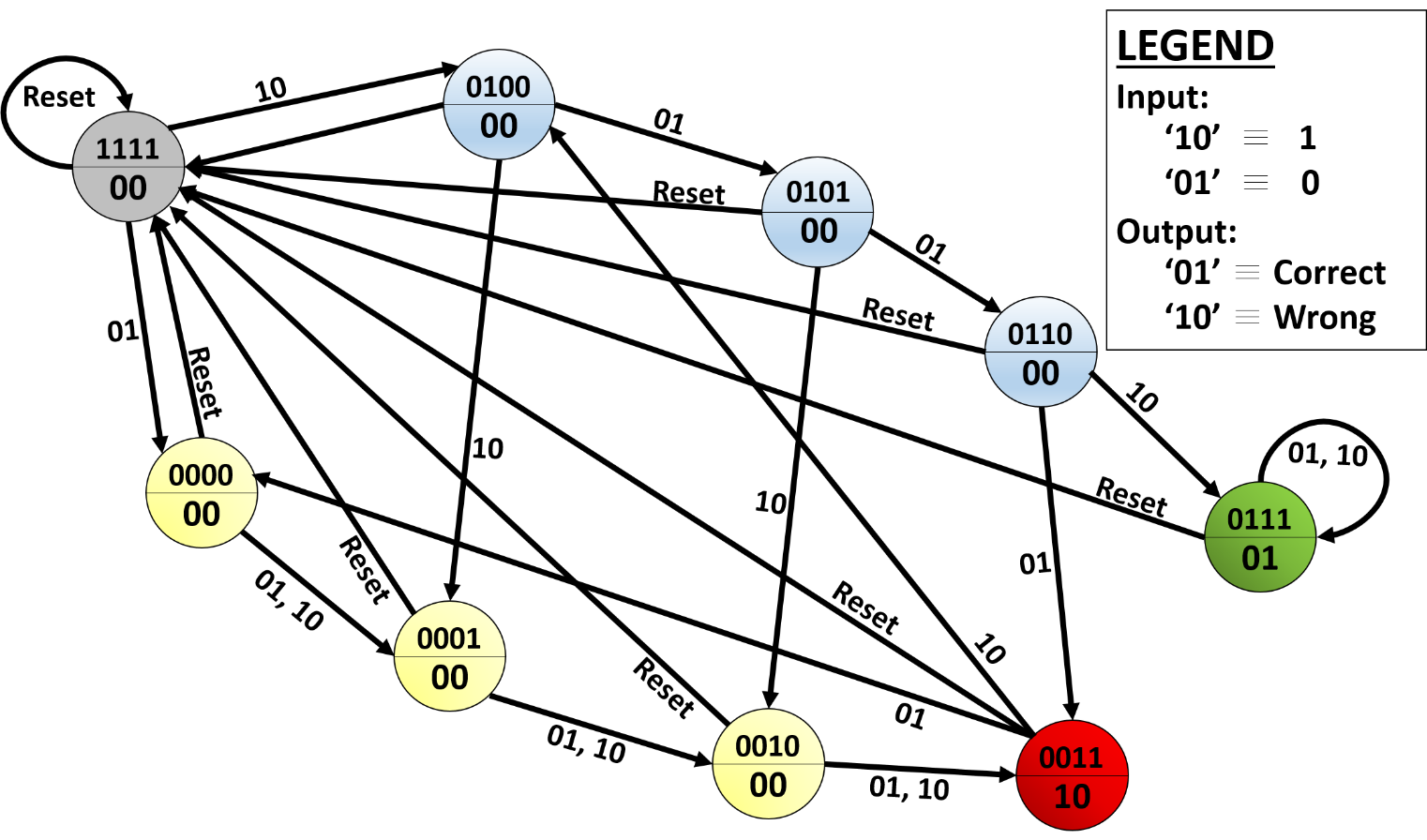
Design a door lock circuit with passcode as “1001”. The code should be entered via 2 Push Buttons: one button for entering 1’s (use **P16**) and another for entering 0’s (use **R16**). Use a third push button (use **T18**) to add reset functionality. Based on the entered code, glow an LED for the following outputs

1. LED 0 (Use pin **T22**) will glow indicating PASS, if the entered 4-digit code is correct
2. LED 1 (Use pin **T21**) will glow indicating FAIL, if the entered 4-digit code is incorrect

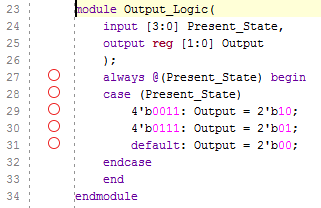
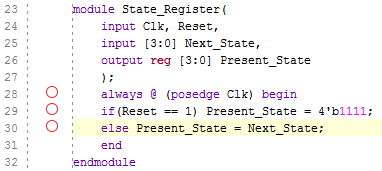
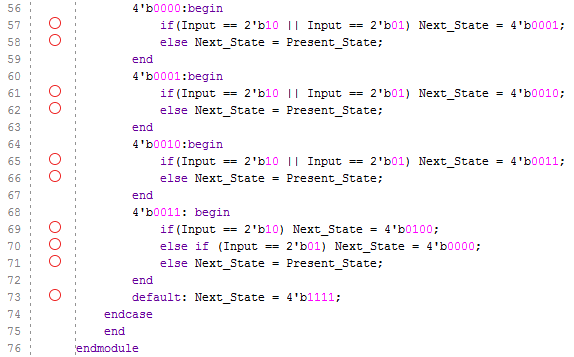
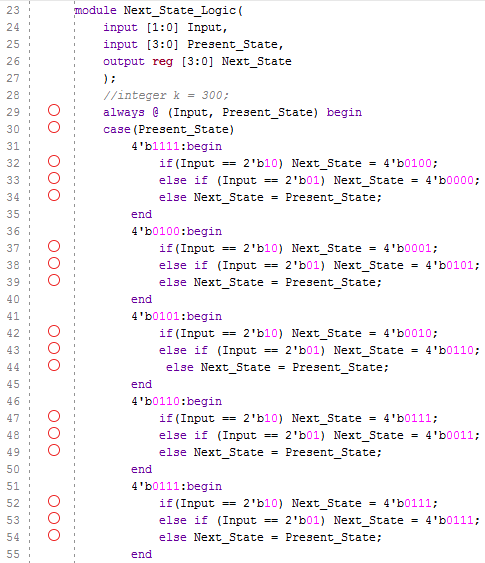
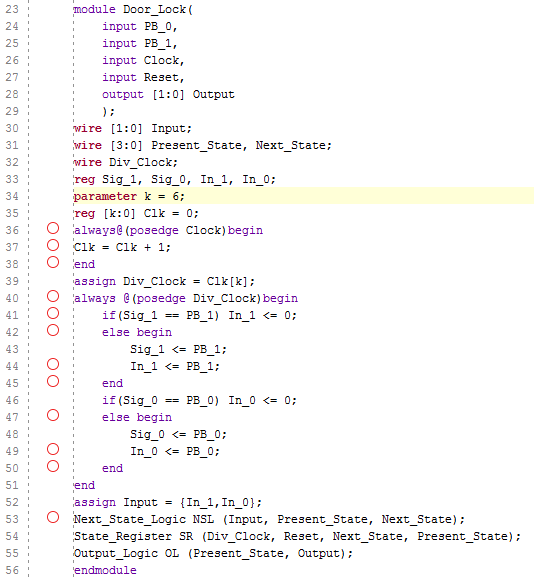
[Note: Digital debouncing has to be implemented for all push button switches]

NAME- **Digvijay Singh** ID Number- **2017AAPS0317H**

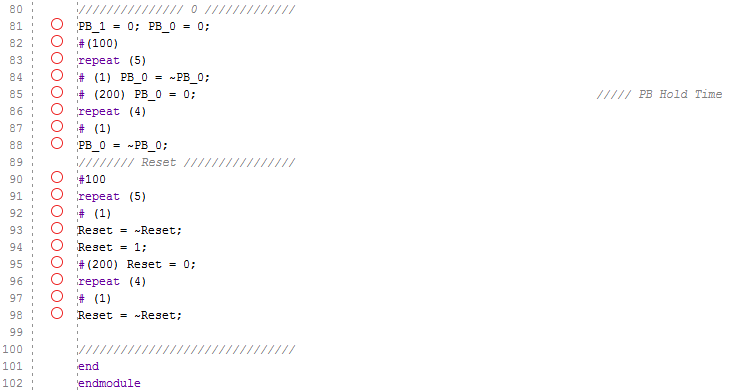
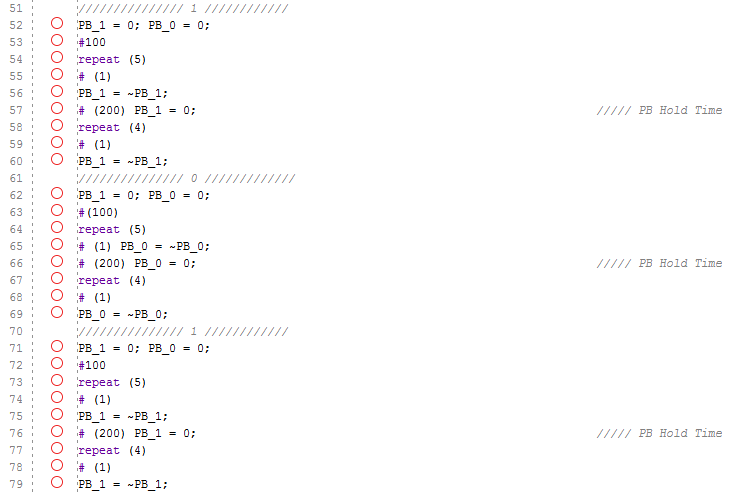
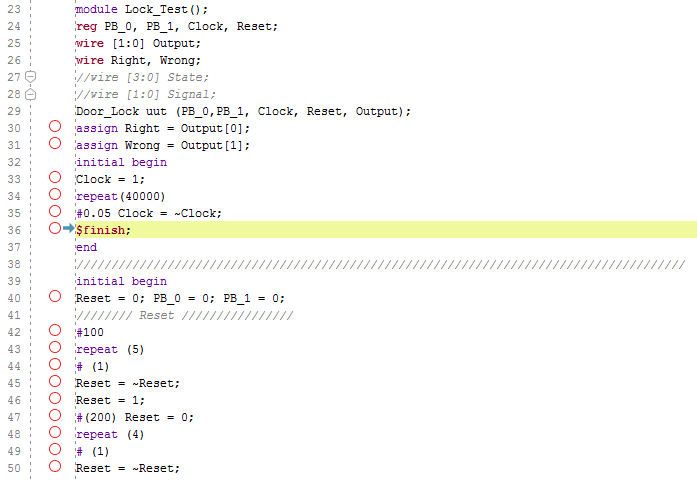
1. **Copy the image of FSM for the above specification (Clearly label all inputs and outputs).**

Answer: 

1. **Copy the image of all your Verilog (main and sub modules) Codes below.**

Answer:1 Main module, 3 sub-modules. (Please see next page)

1. **Copy the image of Test Bench Verilog code below.**

Answer: (See next page)

1. Implement the design on FPGA after including clock division (Elaborate, I/O Plan, Synthesize, Implement, Bitstream and Program) and verify the outputs. Please use the same pins mentioned above for inputs and outputs.
2. **Check the output on FPGA.**
3. **Show the output to the instructor.**
4. **Submit a Zipped folder with file name as <Student\_ID\_No>.zip through Google classroom before due date. The zipped folder should contain the following**

**1) Completed Document**

**2) All source files (design, Test Bench and Constraints)**

**3) Bitstream file**